Amendments to the Claims

The listing of claims below will replace all prior versions and listings of claims in the application.

1. (Original) A transceiver, comprising:

a plurality of pads, wherein at least one of said plurality of pads is a programmable IO pad capable of supporting at least two data protocols and at least two electrical specifications, wherein at least one of said plurality of pads is a programmable MDIO pad capable of supporting at least two data protocols and at least two electrical specifications; and

a plurality of ports in communications with said plurality of pads, wherein one of said plurality of ports is a parallel port in communications with said programmable IO pad.

2. (Original) The transceiver of claim 1, wherein said data protocols and electrical specifications comprise the standards specified in IEEE 802.3™ clause 45 and IEEE 802.3™ clause 22.

3. (Original) The transceiver of claim 1, wherein said data protocols include at least two of XGMII, TBI, RTBI data protocols, wherein said electrical specifications include at least two of HSTL, SSTL, and LVTTL electrical specifications.

4. (Original) The transceiver of claim 1, further comprise:

a bus structure for separating a power connection of said programmable MDIO pad from a power connection of said programmable IO pad.

5. (Original) The transceiver of claim 4, wherein said power connection of said programmable MDIO pad operates at a first voltage and said power connection of said programmable IO pad operates at a second voltage, wherein said first voltage differs from said second voltage.

6. (Original) The transceiver of claim 4, wherein said power connection of said programmable MDIO pad operates at 1.2 volts or 2.5 volts, and said power connection of said programmable IO pad operates at 2.5 volts or 3.3 volts.

7. (Original) The transceiver of claim 1, wherein said programmable IO pad is programmable to operate as an input or an output.

8. (Currently Amended) The transceiver of claim 1, wherein said programmable IO pad is programmable to receive or send ~~at least~~ one of a data signal ~~and~~ or a clock signal.

9. (Original) The transceiver of claim 1, wherein one at least of said plurality of ports is a serial port in communications with said programmable IO pad.

10. (Original) The transceiver of claim 9, wherein said serial port is XAUI.

11. (Original) The transceiver of claim 9, further comprising a bus connecting said parallel port to said serial port on a common substrate with said plurality of ports.

12. (Original) The transceiver of claim 11, wherein said bus is configured to have a ring shape.

13. (Original) The transceiver of claim 11, wherein said bus is configured to have a ring shape around a logic core.

14. (Currently Amended) The transceiver of ~~claim~~ claim 11, further comprising a packet bit error rate tester (BERT) connected to said bus, said packet BERT able to determine bit error rates of at least one of said ~~multiple~~ parallel ~~ports~~ port and said ~~multiple~~ serial ~~ports.~~ port.

15-19. (Canceled)

20. (New) The transceiver of claim 1, wherein the plurality of pads and the plurality of ports are formed on a chip.